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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/972,428	10/05/2001	Christophe Pierrat	NMTI 1002-4	3974

30437 7590 03/01/2004

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EXAMINER	
RUGGLES, JOHN S	

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

5/1

Office Action Summary	Application No.	Applicant(s)	
	09/972,428	PIERRAT ET AL.	
	Examiner	Art Unit	
	John Ruggles	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26 and 28-56* is/are pending in the application.

4a) Of the above claim(s) *1-22* is/are withdrawn from consideration.

5)☒ Claim(s) *32 and 35* is/are allowed.

6)☒ Claim(s) *23-26,28-31,33,34 and 36-56* is/are rejected.

7)☒ Claim(s) *56* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-22 remain withdrawn as nonelected; claims 23-25, 28-32, 35-36, 38, 44-46, 48, and 53-54 have been currently amended; claim 27 has been canceled; and claim 56 has been currently added. Therefore, only claims 23-26 and 28-56 remain under consideration.

Election/Restrictions

Applicants have affirmed the previous election without traverse of Group III, claims 23-55 on page 18 of the amendment filed 19 August 2003. Accordingly, claims 1-22 remain withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to non-elected inventions.

Specification

The previous objections to the specification have been overcome by amendments thereto. Accordingly, these previous objections are now withdrawn.

Claim Objections

The previous objections to the claims have also been overcome by amendments thereto, so these previous objections to the claims are also now withdrawn.

However, the addition of new claim 56 has necessitated another new objection, as stated below.

Claim 56 is objected to because of the following informalities: in lines 3-4, "memory devices defined" should be rewritten as --memory devices are defined--, in order to be

grammatically correct (note that this proposed wording is already found in lines 3-4 of currently amended claim 45). Appropriate correction is required.

Claim Rejections - 35 USC § 112

The previous rejection of claims 24, 45, and 53 under the first paragraph of 35 U.S.C. 112 has been overcome by amendments to these claims in accordance with the examiner's previous suggestion for interpretation of these claims. Therefore, this previous rejection of claims 24, 45, and 53 is now withdrawn.

While most of the previous rejection of claims 23-35, 38, 45, and 53 under the second paragraph of 35 U.S.C. 112 has been overcome by claim amendments, the remaining portion of this previous rejection is restated below. Also, applicants' addition of new claim 56 has necessitated a new rejection under this section, which is similar to the remaining portion of the previous rejection and is incorporated therein, as shown below.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 45, 53, and 56 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

In claim 45 at line 7, in claim 53 at line 7, and in claim 56 at line 6, "the critical path" lacks antecedent basis; also, in claim 53 at line 5 and in claim 56 at line 4, "the floorplan" lacks antecedent basis. Claims 45, 53, and 56 must be amended in response to this rejection.

Claim Rejections - 35 USC § 102

The previous rejection of claims 36-38 and 48-52 under 35 U.S.C. 102(b) as being anticipated by Spence (US Patent 5,573,890) is hereby withdrawn, especially in view of applicant's current amendments to claims 36 and 48 and accompanying clarifying remarks. Instead, these claims have now been incorporated into a revised obviousness rejection, as stated below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 23-26, 28-30, 36-38, 40-41, 45-46, 48-54, and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spence (US Patent 5,573,890) in view of Jinbo, et al. ("0.2 μm or Less Lithography by Phase-Shifting-Mask Technology", 1990, IEEE, pages 33.3.1-33.3.4).

Spence teaches a photolithography (an optical lithography) process of manufacturing an integrated circuit (IC) having a gate pattern using a phase shift mask (PSM) pattern to expose a

resist layer on a wafer (understood to encompass forming a resist layer on a wafer in a first process station (e.g., for coating resist on wafer, etc.) and subsequently moving the resist coated wafer to a second process station (optical lithography system stepper shown in Figure 2(e)) for patterned exposure of the resist). The PSM is designed to reliably shrink gate size for logic circuits (column 4, lines 37-38). The process of manufacturing the circuit involves exposing (defining and exposing in a single step) a resist layer through the patterned PSM shown in Figure 6 to make the circuit shown in Figure 3 (column 5, lines 40-44). Alternatively, a two step exposure process involving first exposure (by a first dose of radiation using a first setting of optical parameters) of the resist through the patterned PSM of Figure 7 followed by second exposure (by a second dose of radiation using a second setting of optical parameters, but is silent as to whether or not the settings for second optical parameters used for the second exposure dose are substantially the same as the first settings for optical parameters used for the first exposure dose) through the patterned trim mask of Figure 8 to remove unwanted dark lines (clearing phase shifting artifacts) described at column 5, lines 45-59. The gate shrink feature shown in Figure 11(b) was manufactured with a wafer stepper exposure apparatus (optical lithography system) such as that shown in Figure 2(e) using either (1) the natural dark line formed by abutting 0° and 180° phase shift regions on the PSM (column 6, lines 30-32) or (2) a narrow opaque line 75 on the mask to overlay the natural dark abutting transition between 0° and 180° phase shift regions on the PSM (column 6, lines 36-42). In order to make this gate shrink feature, column 6, lines 33-36 specify setting the following optical parameters of the optical lithography system: numerical aperture, wavelength of exposure radiation, and light source partial coherence (instant claim 37 for partial coherence (σ); instant claim 38 for numerical aperture (NA); instant claim 48

for numerical aperture, wavelength of radiation, and/or (partial) coherence; instant claim 49 for numerical aperture and partial coherence; instant claim 50 for numerical aperture and/or partial coherence; instant claim 51 for partial coherence as the coherence parameter; and instant claim 52 for different dosage levels).

Spence does not teach that the PSM defines substantially the entire integrated circuit (IC) pattern or that the values for settings of optical parameters are substantially the same while exposing the resist by the PSM and trim mask patterns. Spence also does not teach setting optical parameters including illumination configuration and/or defocus of the exposure radiation.

Jinbo describes a lithography process using PSMs (having phase-shifter edge lines (PEL)) "which basically consist of only shifter patterns" (taken to be referring to "full phase shift" or "full phase" masks defining substantially all of a circuit pattern, found in the 4th paragraph (¶) of the Introduction section at the 2nd column on page 33.3.1 (instant claim 24). This also reads on: instant claim 25 for at least 95% of the overall pattern defined by a PSM; instant claims 45, 53, and 56 for at least 90% of the overall pattern defined by a PSM, all features in the critical path (features having a critical dimension (CD)) defined by a PSM, and/or all features that are not phase shifted due to phase conflicts defined by a PSM; and instant claims 46 and 54 for a pattern characterized by having at least 95% of the overall pattern defined by a PSM. The resulting light intensity pattern formed by the PEL is found to be "shaper" (understood to mean --sharper--) than that obtained from a chrome mask (binary mask, non-PSM) in a stepper optical exposure system (instant claim 26 for a stepper) when compared under the same illumination conditions (illumination configuration, instant claim 40) or substantially the same illumination conditions (substantially the same values for settings of optical parameters

that control characteristics of exposure, instant claims 23, 36, and 48). Substantially the same setting of optical parameters reads on "within plus or minus 10%", instant claim 30). The following illumination conditions (optical parameter settings) had substantially the same values to allow comparison: numerical aperture, exposure wavelength, coherence factor (partial coherence), and/or defocus position (defocus, page 33.3.1, in the 2nd column, under the Concept of a Phase-shifter Edge Line Mask section; instant claims 28-29 and 40-41). The use of PSM lithography is expected to meet the drive toward denser and higher-speed devices (e.g., DRAM, etc.) by improving resolution of substantially all photolithographic patterns (which includes those for memory and/or non-memory devices; reads on instant claims 45, 53, and 56 for at least 80% of the non-memory device portions of the overall pattern defined by a PSM) as explained in the Introduction and Conclusion sections, found in the 1st column on page 33.3.1 and in the 2nd column on page 33.3.2, respectively.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PSM and trim mask photolithography process (by single or plural separate exposures) taught by Spence for shrinking a transistor gate in an IC with the full PSM lithography process to define substantially all of the circuit pattern (including those for memory and/or non-memory devices) using substantially the same values of exposure illumination optical parameter settings for PSM and trim (binary) mask exposures as described by Jinbo. This is because the PSM pattern features are sharper (have better resolution) than those obtainable with only a binary mask as explained by Jinbo to meet the drive toward denser and higher-speed devices (e.g., DRAM, non-memory devices, etc., by allowing definition of smaller feature size patterns). Even though not expressly using both PSM and trim mask exposures together, Jinbo

shows the feasibility of using substantially the same values of optical parameter settings for each of these types of masks. One of ordinary skill in the art would expect to save time between the first PSM exposure and the second trim mask exposure of Spence by keeping the same values of settings for optical parameters (as taught by Jinbo) between these exposures.

Claims 25, 45-46, 53-54, and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spence and Jinbo as applied above, and further in view of Wong, et al. ("Investigating Phase-Shifting Mask Layout Issues Using a CAD Toolkit", 1991, IEEE, pages 27.4.1-27.4.4).

While teaching at least some portion of all the limitations found in claims 25, 45-46, 53-54, and 56 as pointed out above for a PSM and trim mask photolithography process (by single or plural separate exposures to pattern a resist layer on a wafer) in which the PSM is a full PSM defining substantially the entire overall pattern, Spence and Jinbo do not specify a lower percentage of the overall pattern defined by the PSM or address how to resolve phase conflicts when they arise (possibly preventing 100% of the overall pattern from being defined by a PSM).

Wong shows CAD layout of a PSM for a photolithography process to pattern a mask layer (e.g., resist on a wafer, etc.) for manufacturing a DRAM having a non-regular cell pattern in which at least 94% of the patterned cell area is easily shiftable (defined) using two phases (for the PSM, to shrink pattern dimensions by defining at least 94% of the overall pattern by a PSM) and recommends solutions for remaining difficult areas (to define a larger percentage of the overall pattern by imaging through a PSM, according to the abstract in the 1st column on page 27.4.1). Also in the first column on page 27.4.1, the 2nd ¶ of the introduction describes the

shaded areas of Figure 1 to be phase conflict areas (remaining difficult areas) in which closely spaced geometries have the same phase, making up about 1% of the total cell area and about 6% of the edges. The conflict areas are reduced by CAD analysis and redesign to eliminate some of the phase conflicts (allowing these conflict areas of the overall pattern to still be reduced in size (shrunk) by use of a PSM) or at least partially convert the conflict areas to conflict-free areas (e.g., by using additional phases in these areas of the PSM, etc.). These methods reduce the violation (difficult or phase conflict) area and further increase chip shrinkage (to increase the proportion of the overall pattern defined by a PSM to greater than 94%), as described in the last ¶ of the DRAM Investigation Results section found in the 1st column on page 27.4.2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PSM and trim mask photolithography process (by single or plural separate exposures) taught by Spence and Jinbo for shrinking a circuit with at least 94% of the overall pattern defined by the PSM designed by CAD as shown by Wong (encompasses instant claims 25, 46, and 54 for at least 95% of the overall pattern defined by a PSM; reads on instant claims 45, 53, and 56 for at least 80% of the non-memory device portions of the overall pattern defined by a PSM, at least 90% of the overall pattern defined by a PSM, and all the features in the overall pattern defined by a PSM except those not phase shifted due to phase conflicts; and renders obvious instant claims 45, 53, and 56 for all the features in the critical path (critical dimensions, CD) of the overall pattern defined by a PSM, and/or everything in the overall pattern except test and/or dummy structures (not critical) defined by a PSM). This is because the PSM pattern features increase chip shrinkage by decreasing pattern dimensions. Therefore, the highest percentage of the overall pattern that can be defined by PSM features (e.g., by reducing phase

conflicts in difficult areas, etc.) during photolithography will be expected to result in the greatest overall dimension reduction.

Claims 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spence and either Jinbo or Wong as applied above, and further in view of Pierrat (US Patent 6,040,892).

While teaching a PSM and trim mask photolithography process (by single or plural separate exposures to pattern a resist layer on a wafer) in which the PSM is either a full PSM defining substantially the entire overall pattern (Jinbo) or a PSM defining at least 94% of the overall pattern (Wong), Spence and either Jinbo or Wong do not specify that the PSM and trim masks are on the same reticle and do not describe blading the PSM and trim masks during exposure to permit different dosing through these masks.

Pierrat discloses optical lithographic techniques (photolithographic processes) for patterned exposure (including multiple exposures to different patterns) of a resist layer on a semiconductor wafer and a corresponding reticle having multiple mask patterns (including PSMs) on the same reticle shown in Figure 1 to form a circuit pattern (column 1, lines 10-15, column 3, lines 39-51, and column 4, lines 4-20; instant claims 27 and 33). As shown in Figure 2 and described at column 4, lines 35-57, the different masks on the reticle 211 are selectively exposed (differently dosed) to project these patterns onto the semiconductor wafer (to image a resist layer on the wafer). The different dosing of the masks is controlled by selective mechanical movement of aperture blades 216, 218, 220, and 222 (blading, instant claim 34) to open a selective area aperture 214 and allow light from the source 212 that has been imaged by at least one of the masks to expose a patterned image area onto the resist. The wafer is moved and

aligned with respect to the masks on the reticle by a conventional stepper 230 (optical lithography system). Multiple exposures through different masks (including a PSM) allow undesired imaged lines (phase shifting artifacts) in the pattern to be removed (phase shift artifacts are cleared) by a second complementary or trim mask exposure overlapping these undesired lines before further processing (developing) of the resist image (column 5, line 54 to column 6, line 12). Placing the masks on a single reticle simplifies alignment and saves cost when manufacturing complex circuits and devices (column 5, lines 1-4 and 24-28). Moving and/or sizing the aperture by blading controls which image is projected and where it is projected (column 5, lines 5-7 and 29-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PSM and trim mask photolithography process (by single or plural separate exposures) taught by Spence and either Jinbo or Wong with use of the PSM and trim mask on a single reticle which are differently dosed by blading as disclosed by Pierrat. This is because placing the masks on a single reticle simplifies alignment in the stepper and blading allows moving and sizing of the projection aperture. It would also have been obvious to change the exposure intensity or dosage by controlling the time period over which the aperture is open for each mask pattern (which is understood to be a well known function for a camera aperture) to prevent imaging of unwanted phase shifting artifacts.

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Spence and Jinbo as discussed above, and further in view of either Pierrat or Borodovsky (US Patent 5,424,154).

While teaching a PSM and trim mask photolithography process (by single or plural separate exposures), Spence and Jinbo do not teach a specific dosing ratio (or point out reasons for using a different dosing ratio) for the PSM and trim mask exposures which satisfies the ratio of 1.0 to r where $r > 0$.

The teachings of Spence and Pierrat are discussed above.

Borodovsky teaches a lithographic process for making a semiconductor device (e.g., logic circuit transistor gate structure, etc.) with enhanced resolution by either exposure of a resist layer through a PSM (and then a complementary or trim mask) or using oblique illumination (off-axis exposure at an oblique angle to the resist rather than the 90° angle conventionally used – this suggests a purpose for setting the exposure radiation axis of propagation at the resist layer and the illumination configuration (depending on the light source) during exposure) to expose a mask pattern on a resist layer (column 1, line 47 to column 2, line 7). In the PSM alternative, the first PSM exposure is followed by a complementary or trim mask exposure (column 4, line 3 to column 5, line 61). The resolution of the imaged pattern is shown to depend on optical lens numerical aperture and wavelength of exposure radiation at column 1, lines 20-31. Periodic structures are reproduced with increased resolution and typically have less variation in linewidth due to varying defocus (column 2, lines 36-38). These statements suggest reasons for setting optical parameters during exposure to include the following: lens numerical aperture, wavelength, illumination configuration, defocus, and axis of propagation at the resist layer. The importance of using a complementary or trim reticle or mask in improving contrast (enhancing resolution) increases as the feature size decreases (column 8, lines 21-23). Borodovsky specifically points out that at smaller dimensions, the exposure doses for both reticles or masks

must be adjusted or different to provide for complete exposure of the spaces without overexposure of the lines for a resulting composite intensity or total exposure dose having sufficient contrast (column 8, lines 31-40). The exposure dose for each mask depends on the specific lithographic process and features being formed, and some experimentation with exposure parameters for both reticles or masks may be necessary to achieve acceptable resolution (column 8, lines 35-40). This is taken to mean that the setting of a dosing ratio between first exposure through the PSM and second exposure through the complementary or trim mask is highly dependent on the overall configuration in the optical lithography system, in order to obtain the best resolution. Therefore, setting of only the dosing ratio without also specifying appropriate limitations for all other relevant optical parameters would not ensure the best resolution.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PSM and trim mask photolithography process (by single or plural separate exposures) as taught by Spence and Jinbo with adjusted or different dosing for the PSM and trim mask exposures as taught by either Pierrat or Borodovsky. This is in order to either (1) allow appropriate exposure through different sized bladed apertures as disclosed by Pierrat or (2) improve pattern resolution by providing complete exposure of pattern spaces without overexposure of pattern lines for a resulting composite intensity or total exposure dose having sufficient contrast as pointed out by Borodovsky. This renders obvious at least a portion of the dosing ratio for the PSM and trim mask exposures which satisfies the ratio of 1.0 to r where $r > 0$ as specified in instant claim 31 (e.g., even the same dosing ratio for PSM to trim mask exposures reads on this range and would be expressed as 1:1 or 1.0 to r where $r = 1.0$, etc.).

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Spence and Jinbo as discussed above in view of Borodovsky.

The combined teaching of Spence and Jinbo discussed above is drawn to a PSM and trim photolithography process including setting numerical aperture and partial coherence, but does not specifically include setting the following exposure radiation parameters: illumination configuration, defocus, and axis of propagation at the resist layer.

The teaching of Borodovsky is discussed above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PSM and trim mask photolithography process (by single or plural separate exposures) involving setting of optical parameters including numerical aperture and partial coherence as taught by Spence and Jinbo with setting of additional optical parameters including illumination configuration, defocus, and axis of propagation of exposure radiation at the resist layer as taught by Borodovsky to obtain better contrast and enhance resolution as explained by Borodovsky.

Claims 43-44, 47, and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spence and Jinbo as discussed above in view of Pierrat (US Patent 6,040,892).

While teaching a PSM and trim mask photolithography process (by single or plural separate exposures to pattern a resist layer on a wafer), Spence and Jinbo do not specify that the PSM and trim masks are on the same reticle and do not describe blading the PSM and trim masks during exposure to permit different dosing through these masks. Spence and Jinbo also do not

point out that a value for an optical parameter setting is changed by mechanical adjustment of an optical element.

The teachings of Spence, Jinbo, and Pierrat are discussed above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PSM and trim mask photolithography process (by single or plural separate exposures) taught by Spence and Jinbo with use of the PSM and trim mask on a single reticle or mask (instant claim 44) which are differently dosed (instant claim 43) by blading as disclosed by Pierrat. This is because placing the masks on a single reticle simplifies alignment in the stepper and blading allows moving and sizing of the projection aperture (it would also have been obvious to change the exposure intensity or dosage by controlling the time period over which the aperture is open for each mask pattern, which is understood to be a well known function for a camera aperture, to prevent imaging of unwanted phase shifting artifacts). Furthermore, it would have been obvious to change at least one value of an optical parameter setting in the Spence and Jinbo process by mechanical adjustment of an optical element, because a blading aperture was mechanically moved or sized (affecting the overall optical configuration) as disclosed by Pierrat (instant claims 47 and 55).

Allowable Subject Matter

The previous objection of claims 32 and 35 is hereby withdrawn as overcome by current amendments to these claims. Accordingly, claims 32 and 35 are now allowed as currently amended.

The following is an examiner's statement of reasons for allowance of claims 32 and 35: while the concept of different dosing between the PSM exposure and subsequent overlapping trim mask exposure of a resist layer in integrated circuit (IC) manufacture to obtain the smallest features with the best resolution are not new, the specific dosing ratio of 1.0 (for the PSM) to r (for the trim mask) where 2 <= r <= 4 of instant claim 32 and, more specifically, 1:2 (PSM:trim mask) of instant claim 35 are both distinguished over the prior art (which does not teach these specific ratios).

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Response to Arguments

Applicants' arguments regarding the previous objection of claims 32 and 35 as being previously dependent on rejected base claims have been fully considered and are persuasive in view of current amendments to these claims, which have now been presented in independent form including all of the limitations of the base claim and any intervening claims. Therefore, this previous objection to these claims has been withdrawn and claims 32 and 35 have now been allowed for the reasons indicated above.

The previous objections to the specification have now been withdrawn as having been overcome by amendments thereto.

The previous objections to the claims have also been withdrawn as having been overcome by amendments thereto. However, the addition of new claim 56 has necessitated another new objection, which is set forth above.

While most of the previous rejection of claims 23-35, 38, 45, and 53 under the second paragraph of 35 U.S.C. 112 has been overcome by claim amendments, the remaining portion of this previous rejection has been restated above along with incorporation of a new rejection necessitated by new claim 56.

Applicants' arguments with respect to claims 23-26, 28-31, 33-34, and 36-56 have been fully considered but are moot in view of the revised ground(s) of rejection, particularly as necessitated by current amendments to the claims. However, no new art has been cited and these rejections are now made FINAL.

Conclusion

Applicant's amendment necessitated the new ground(s) of objection and rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Ruggles whose telephone number is 571-272-1390. The examiner can normally be reached on Monday-Thursday and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John Ruggles
Examiner
Art Unit 1756

MARK F. HUFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700